## REMARKS/ARGUMENTS

Claims 1-6 and 15-26 are currently pending in the present patent application, with claims 7-14 and 27-30 having been cancelled through the above claim amendments.

In the Office Action, the Examiner rejected claim 5 under 35 U.S.C. § 112 for including the phrase "for example." Claim 5 has been amended to remove this phrase, eliminating any deficiencies under Section 112. It should also be noted that while claims 7-14 and 27-30 may be allowable over the art of record, the first page of the Office Action erroneously indicates these claims as allowed even though they are nonelected claims pursuant to a previously filed response to restriction requirement. The Examiner made the restriction final in the Office Action and thus these claims have been cancelled. Also note that some of the claims have been amended to replace the phrase "characterized in that" with the term "wherein." This has been done only because this latter term is an accepted and frequently construed term under U.S. patent laws. These amendments conform the claims with accepted U.S. practice and do not narrow the scopes of the amended claims.

The Examiner rejected claims 1-6 and 15-26 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,614,748 to Nakajima *et al.* ("Nakajima") in view of U.S. Patent No. 6,800,940 B2 to Catabay *et al.* ("Catabay"). The Catabay patent is relied upon for disclosing a layer having a dielectric constant between 1 and 3.9.

Before addressing the Examiner's rejections of claims 1-6 and 15-26, the disclosed embodiments of the invention will first be discussed in comparison to the applied references in order to help the Examiner appreciate certain distinctions between the pending claims and the subject matter of the applied reference. Specific distinctions between the pending claims and the applied reference will be discussed after the discussion of the disclosed embodiments and the applied reference. This discussion of the differences between the disclosed embodiments and applied reference does not define the scope or interpretation of any of the claims.

An embodiment of the present invention is illustrated in Figures 6 and 7. These figures show what are termed a vertical sectional views. These views are in what is termed the "width" direction or plane in the present patent application, meaning they are in the plane of a given row of memory cells in a memory-cell array. Thus, in Figures 6 and 7 the field oxide FOX regions are formed between nonvolatile memory cells in a given row of memory cells. As shown in Figures 6 and 7, floating gates FG of adjacent memory cells in

the given row or along the width direction are shown. A low k dielectric constant layer 9 is formed between the two floating gates FG, which reduces electrical coupling between adjacent floating gates. In the width direction, which corresponds to a direction parallel to a word line associated with a given row of memory cells, segments of the low k dielectric constant layer 9 separate the floating gates FG of adjacent memory cells in this row. The low k dielectric constant layer separates floating gates of memory cells in respective rows of a memory cell array.

In contrast to the embodiment of Figures 6 and 7, Figure 1 of Nakajima illustrates a view of adjacent nonvolatile memory cells not in the width direction or plane but instead in the "length" view or plane as this term is used in the present application. The length direction corresponds to the direction along a column of memory cells or a direction orthogonal to the width direction. In fact, Figure 4D in Nakajima is in the width direction (only Figures 4A-4D appear to illustrate the Nakajima invention in the width direction) and when this figure is compared to Figure 1c of the present application it is seen that these figures are the same. The structures of these two figures do not include any low k dielectric constant layer between adjacent floating gate regions. In Figure 4D of Nakajima the second polysilicon layer 12 forms the control gate of memory cells in the illustrated row and only this layer is between adjacent floating gate regions 8.

Nakajima is concerned with the formation of a special dielectric layer with good lateral electrical insulation capability towards the source and drain areas of the cell, which as just described is along the length direction. Nakajima is not directed to electrical insulation between adjacent floating gate along the width direction, which is the direction perpendicular to the direction dealt with in Nakajima. Moreover, Nakajima is directed to the prevention of current leakage, which results in utilization of phosphorous doped oxide, which does a low k dielectric constant.

The Catabay patent is directed reduction of capacitive effects among metal lines in an integrated circuit and is directed to the problem of insulating metal lines to avoid the problem of via poisoning. The use of low k dielectric reduces such capacitive coupling. Catabay discloses the deposition of a low k dielectric layer between the metal stripes and a different composition low k dielectric layer on top of the stripes. In embodiments of the present invention as just described, a low k material is formed only between the floating

gates and a high k material is contained on top in order to increase the capacitive coupling between floating gate and control gate, which is contrary to the Catabay structure.

Claim 1 recites a non-volatile memory cell integrated on a semiconductor substrate. The memory cell includes a floating gate transistor including a source region and a drain region. A gate region projects from the substrate and is comprised between said source and drain regions, the gate region having a predetermined length and width and comprising a first floating gate region and a control gate region. The floating gate region is insulated laterally, along the width direction, by a dielectric layer with low dielectric constant value. Neither Nakajima nor Catabay, whether taken singly or in combination, discloses or suggests a floating gate region that is insulated laterally, along the width direction, by a dielectric layer with low dielectric constant value. Figure 1 illustrates a direction orthogonal to the width direction, and thus does not have anything to do with the recited structure. Moreover, Figure 4D of Nakajima similarly does not disclose or suggest a low k dielectric constant layer to separate floating gates in the width direction, *i.e.*, to separate floating gates of adjacent memory cells in a given row of memory cells. The combination of elements recited in claim 1 is therefore allowable.

Claim 15 recites a memory cell matrix formed on a semiconductor substrate comprising a plurality of memory cells organized in rows and columns, each cell being formed according to claim 1, the cell matrix being wherein adjacent memory cells belonging to a same row of said memory cell matrix are insulated from each other by a dielectric layer with low dielectric constant value. As previously described, Figure 1 of Nakajima neither discloses nor suggests adjacent memory cells belonging to a same row of a memory cell matrix being insulated from each other by a dielectric layer with low dielectric constant value. Figure 1 does not show adjacent memory cells of a same row but instead is in the length direction perpendicular to the width direction, which is along the direction of adjacent memory cells in the same row. Accordingly, the combination of elements recited in claim 15 is allowable.

Claim 16 recites a memory-cell structure formed on a semiconductor substrate and including a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate. Each memory cell includes a floating gate region and the memory-cell structure includes an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows

of the structure. Nakajima simply does not disclose or suggest a memory-cell structure including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the structure. Once again, Figure 1 illustrates a direction orthogonal to the width direction, and thus does not have anything to do low k dielectric regions formed between floating gate regions of memory cells in respective rows of a memory-cell structure. Figure 4D of Nakajima similarly fails to disclose or suggest a low k dielectric constant layer separating adjacent floating gates of memory cells in respective rows of a memory-cell structure. The combination of elements recited in claim 16 is therefore allowable.

Independent claims 21 and 24 are allowable for reasons similar to those just set forth for claim 16. All dependent claims are allowable for at least the same reasons as the associated dependent claims and due to the additional limitation added by each of these dependent claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

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